In re Patent Application of: Kazuaki Kurihara et al.

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For: LAYER CAPACITOR ELEMENT AND PRODUCTION PROCESS AS WELL AS ELECTRONIC DEVICE

TRANSLATOR'S DECLARATION

Honorable Commissioner of Patents & Trademarks
Washington, D.C. 20231

Sir:

I, Keizo Komoriya, residing at c/o A. AOKI, ISHIDA & ASSOCIATES, Toranomon 37 Mori Bldg., 3-5-1, Toranomon Minato-ku, Tokyo 105-8423, Japan declare the following:

(1) That I know well both the Japanese and English languages;

(2) That I translated Japanese Patent Application No. 2002-330578, filed November 14, 2002, from the Japanese language to the English language;

(3) That the attached English translation is a true and correct translation of the aforesaid Japanese Patent Application No. 2002-330578 to the best of my knowledge and belief; and

(4) That all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and that such false statements may jeopardize the validity of the application or any patent issuing thereon.

February 9, 2006

Date

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[TITLE OF THE INVENTION] Thin Layer Capacitor and Process for Its Production

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[TITLE OF THE INVENTION] Thin Layer Capacitor and Process for Its Production

[SCOPE OF CLAIM FOR PATENT]

[CLAIM 1] A thin layer capacitor comprising a capacitor with a dielectric layer made of a metal oxide and a protective insulating layer made of a resin material, characterized in that a barrier layer made of a non-conductive inorganic material is provided between said capacitor and said protective insulating layer.

[CLAIM 2] A thin layer capacitor characterized by comprising:

a capacitor with a dielectric layer made of a metal oxide, formed on a supporting substrate;

a barrier layer made of a non-conductive inorganic material covering at least the top and side of said capacitor, and

a protective insulating layer made of a resin material, formed on said barrier layer.

[CLAIM 3] A thin layer capacitor according to claim 1 or 2, characterized in that said barrier layer has the same composition as that of said dielectric layer.

[CLAIM 4] A thin layer capacitor according to any one of claims 1 to 3, characterized in that said barrier layer is amorphous.

[CLAIM 5] A thin layer capacitor according to any one of claims 1 to 4, characterized in that the terminals for external electrical connection are provided at least at a location other than the edge of one side of the package.

[CLAIM 6] A thin layer capacitor according to any one of claims 1 to 5, characterized in that a plurality of capacitors with different capacitances are provided in a single thin layer capacitor.

[CLAIM 7] A process for production of a thin layer capacitor comprising a capacitor with a dielectric layer made of a metal oxide and a protective insulating layer made of a

resin material, characterized by comprising the steps of:

forming said capacitor;

forming a barrier layer made of a non-conductive inorganic material, situated between said capacitor and said protective insulating layer; and

forming said protective insulating layer situated on said barrier layer.

[CLAIM 8] A process for production of a thin layer capacitor, characterized by comprising the steps of:

forming a capacitor with a dielectric layer made of a metal oxide, formed on a supporting substrate;

forming a barrier layer made of a non-conductive inorganic material covering at least the top and side of said capacitor; and

forming a protective insulating layer made of a resin material, formed on said barrier layer.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[Technical Field of the Invention]

The present invention relates to a capacitor, and more specifically it relates to a thin layer capacitor comprising a capacitor formed on a semiconductor substrate by a thin layer fabrication process.

[0002]

[Prior Art]

The increased processing speeds of LSIs in recent years have led to the development of decouple processing as a strategy for preventing diffusion of high-frequency noise, as well as a demand for improved high-frequency tracking performance of the decoupling capacitors used therefor.

[0003]

To achieve improved high-frequency tracking performance of decoupling capacitors, the decoupling capacitors must have characteristics such as high capacitance and low impedance connections in distributed circuits, and it is known that this

requirement can be achieved by thin layer capacitors having capacitors formed by thin layer fabrication processes on semiconductor substrates.

[0004]

Because such thin layer capacitors are miniature, have large capacities and are excellently suited for microprocessing, they allow connections with circuit boards to be formed as bump connections with narrow pitches between terminals, thereby reducing mutual inductance and making possible effective functioning for low-inductance connections with LSIs.

[0005]

However, since miniature size and large capacity of a thin layer capacitor is achieved by using a metal oxide as the dielectric material, the metal oxide undergoes reduction during the fabrication process and thereby produces deterioration in the characteristics.

[0006]

In order to solve this problem of deterioration of dielectric materials, the following has been proposed, for example, in Japanese Unexamined Patent Publication (Kokai) No. 2000-49311 referred to as Patent Document 1.

[0007]

Figs. 8 and 9 show in detail the separate steps of a conventional process for production of a thin layer capacitor introduced in the aforementioned patent publication.

[0008]

First, as shown in Figs. 8(A) and 8(B), a lower electrode 2 made of platinum Pt is formed on a semiconductor substrate 1. Then as shown in Figs. 8(C) and 8(D), a capacitive insulating layer 3 made of an insulating metal oxide and an upper electrode 4 made of platinum Pt are deposited thereover in that order.

[0009]

This is followed by the etching step shown in Fig. 8(E), and then as shown in Fig. 9(F), a protective insulating layer

6 is deposited on the upper electrode 4 so as to completely cover the upper electrode 4.

[0010]

Next follows a resist mask-forming step for formation of a resist mask 9, as shown in Fig. 9(G), and finally contact holes 9 are formed as shown in Fig. 9(H) through a dry etching step (not shown).

[0011]

In the capacitor element described above, the problem of reduction of the capacitive insulating layer due to hydrogen generated in the step of removing the resist mask 10 is prevented by such means as limiting the open area of the contact holes 9 of the protective insulating layer 6 to not more than 5 μm^2.

[0012]

[Patent Document 1] Japanese Unexamined Patent Publication (Kokai) No. 2000-49311 (particularly, paragraphs 0033 to 0036 and Fig. 3)

[0013]

[Problems to be Solved by the Invention]

In a conventional thin layer capacitor as described above, reduction of the insulating metal oxide of the capacitive insulating layer 3 is prevented by blocking it with a protective insulating layer 6.

[0014]

The thin layer capacitor of the invention, however, employs bumps or similar high-precision packing-enabling connection forms (to realize low inductance) for the terminals.

[0015]

With this type of connection form, the mechanical stress generated by the difference in thermal expansion coefficients of the thin layer capacitor and the circuit board on which the thin layer capacitor is mounted can directly bear on the thin layer capacitor terminals, without being mediated by the buffer material, such as a lead.

[0016]

An internal capacitor composed of an extremely thin layer easily tends to undergo a problem such as interlayer peeling due to the aforementioned mechanical stress, and in order to avoid this problem it is essential to use as the protective insulating layer a resin material such as polyimide which absorbs the mechanical stress from bumps, etc.

[0017]

Such a solution, however, results in the following new problems.

[0018]

Firstly, there is the problem of reduction of the dielectric material in the step of forming the protective insulating layer. For example, a polyimide resin varnish forms a polyimide resin when cured at about 400°C, but since the acid anhydride and diamine undergo dehydrating condensation polymerization to generate H_2O during curing of the polyimide varnish as the protective insulating layer, the H_2O decomposes to hydrogen ions and the hydrogen ions reach the dielectric material, thereupon reducing it.

[0019]

This occurs because the H_2O infiltrates the capacitor electrodes in a hydrogen ion state due to the catalytic effect of the platinum Pt composing the electrodes, and the hydrogen ions reach the interface between the electrodes and the dielectric material by diffusion, thereby resulting in oxygen loss of the dielectric material.

[0020]

Secondly, there is a problem which occurs during actual use in the field, though this is not a problem of the production steps illustrated in the prior art example.

[0021]

This problem occurs due to the moisture absorption property of the resin material, whereby due to the high temperature surrounding the thin layer capacitor, moisture in the air absorbed by the polyimide resin migrates to the

internal capacitor under the high temperature and reduces the dielectric material.

[0022]

It is therefore an object of the present invention to provide a thin layer capacitor which solves the problems related to reduction of the dielectric material which occurs when a resin material such as polyimide is used as a protective insulating layer to absorb the mechanical stress from bumps, and which has excellent high-frequency tracking performance and low deterioration of characteristics.

[0023]

[Means for Solving the Problems]

In order to achieve the object stated above, the thin layer capacitor of the invention according to claim 1 is a thin layer capacitor comprising a capacitor with a dielectric layer made of a metal oxide and a protective insulating layer made of a resin material, characterized in that a barrier layer made of a non-conductive inorganic material is inserted between the capacitor and the protective insulating layer.

[0024]

Further, the thin layer capacitor of the invention according to claim 2 is characterized by being provided with a capacitor with a dielectric layer made of a metal oxide, formed on a supporting substrate, a barrier layer made of a non-conductive inorganic material covering at least the top and side of the capacitor, and a protective insulating layer made of a resin material, formed on the barrier layer.

[0025]

According to the construction of claim 1 or claim 2, the protective insulating layer and the internal capacitor are physically separated by the barrier layer. Thus, moisture released from the resin material of the protective insulating layer is prevented from reaching the metal oxide layer constituting the dielectric layer of the capacitor.

[0026]

As a result, it is possible to use as the protective

insulating layer a resin material such as polyimide which absorbs mechanical stress from the bumps, while preventing reduction of the metal oxide dielectric layer material due to moisture released from the resin material.

[0027]

Furthermore, the invention according to claim 3 is a thin layer capacitor of the invention according to claim 2, characterized in that the barrier layer has the same composition as that of the dielectric layer.

[0028]

According to the construction of claim 3, the composition of the material constituting the barrier layer is the same as the composition of the material constituting the dielectric layer, thereby allowing satisfactory layer adhesion to be guaranteed. Also, it is possible to obtain a thin layer capacitor having high reliability for the bonding surface between the dielectric layer and the barrier layer against mechanical stress (that is, the bonded layers are resistant to problems such as peeling).

[0029]

Moreover, the invention according to claim 4 is a thin layer capacitor of the invention according to any one of claims 1 to 3, characterized in that the barrier layer is amorphous.

[0030]

According to the construction of claim 4, it is possible to achieve high reduction resistance of the barrier layer.

[0031]

A crystallized metal oxide is used as the material for the dielectric layer in order to obtain a high dielectric constant. However, since gaps exist between the individual crystal grains of the crystals, migration of hydrogen ions in the crystals is facilitated. It is therefore effective to use an amorphous material, which is resistant to hydrogen ion migration, as a barrier layer to prevent the hydrogen ion migration, and a very high blocking effect against hydrogen

ions can be achieved by a construction using such a material.

[0032]

In addition, the invention according to claim 5 is a thin layer capacitor of the invention according to any one of claims 1 to 4, characterized in that the terminals for external electrical connection are provided at least at a location other than the edge of one side of the package.

[0033]

According to the construction of claim 5, it is possible to reduce the spaces between terminals by forming the terminals at desired locations at the center of the package, even when the capacitor inside the thin layer capacitor has a large form.

[0034]

That is, it is possible to provide a thin layer capacitor having large capacitance and allowing low inductance connections.

[0035]

Further, the invention according to claim 6 is a thin layer capacitor of the invention according to any one of claims 1 to 5, characterized in that a plurality of capacitors with different capacitances are provided in a single thin layer capacitor.

[0036]

According to the construction of claim 6, for example in cases where a plurality of capacitors with different capacitances are necessary, the plurality of capacitors can be mounted as a single package instead of separately, thereby permitting more efficient use of the mounting area on the circuit board onto which the thin layer capacitor 20 is to be mounted.

[0037]

In addition, it is also possible to lower part costs and reduce the number of mounting steps in the part mounting process.

[0038]

Furthermore, the thin layer production process of the invention according to claim 7 is a process for production of a thin layer capacitor comprising a capacitor with a dielectric layer made of a metal oxide and a protective insulating layer made of a resin material, characterized by comprising a step of forming the capacitor, a step of forming a barrier layer made of a non-conductive inorganic material, situated between the capacitor and the protective insulating layer, and a step of forming the protective insulating layer situated on the barrier layer.

[0039]

Moreover, the thin layer capacitor production process of the invention according to claim 8 is characterized by comprising a step of forming a capacitor with a dielectric layer made of a metal oxide, formed on a supporting substrate, a step of forming a barrier layer made of a non-conductive inorganic material covering at least the top and side of the capacitor, and a step of forming a protective insulating layer made of a resin material, formed on the barrier layer.

[0040]

According to the construction of claim 7 or 8, the interior of the protective insulating layer and the capacitor are physically separated by the barrier layer. That is, moisture released from the resin material of the protective insulating layer is prevented from reaching the metal oxide layer composing the dielectric layer of the capacitor.

[0041]

As a result, it is possible to produce a thin layer capacitor which employs as the protective insulating layer a resin material such as polyimide which absorbs mechanical stress from the bumps, while preventing reduction of the metal oxide dielectric layer material due to moisture released from the resin material.

[0042]

[Embodiments for Carrying out the Invention]

(First Embodiment)

A thin layer capacitor according to a first embodiment of the present invention will now be explained with reference to Figs. 1 to 3, in the order of steps (A) to (J) of Figs. 2 and 3 showing the thin layer capacitor production process.

[0043]

(i) Capacitor-forming step

As shown in Figs. 2(A) to 2(D), a lower electrode layer 12 composed of platinum, a dielectric layer 13 composed of a composite oxide and an upper electrode layer 14 composed of platinum Pt are formed in that order on a silicon substrate 11 prepared as the supporting substrate, to form a capacitor 30.

[0044]

A metal oxide with a high dielectric constant is used herein as the material for the dielectric layer 13 to achieve downsizing and large capacitance.

[0045]

Further, a precious metal such as platinum Pt or iridium Ir, having excellent oxidation resistance in high temperature environments and allowing satisfactory crystal orientation control during formation of the dielectric layer 13, is used as the material for the electrodes (the lower electrode layer 12 and upper electrode layer 14) of the capacitor 30.

[0046]

Particularly, the series of production steps may be carried out in the following manner.

[0047]

For the step of forming the lower electrode layer 12 shown in Fig. 2(B), first a silicon wafer is used as the silicon substrate 11, and a sputtering method is used to form films of titanium oxide TiO_2 (20 nm) and platinum Pt (100 nm) in that order on the silicon wafer. The titanium oxide TiO_2 (20 nm) can serve the role of an adhesion layer between the silicon Si and platinum Pt.

[0048]

In this step, the sputtering conditions for the titanium oxide TiO_2 are a substrate temperature of 500°C, an RF power

of 200 W, a dielectric coil power of 30 W, a gas pressure of 0.1 Pa and an Ar/O_2 ratio of 7/1.

[0049]

Further, the sputtering conditions for the platinum Pt are a substrate temperature of 400°C, a DC power of 100 W, a dielectric coil power of 30 W and a gas pressure of 0.1 Pa.

[0050]

In the step of forming the dielectric layer 13 shown in Fig. 2(C), an oxide $(Ba_x, Sr_{1-x})TiO_3$ (hereinafter referred to as "BST") comprising barium Ba, strontium Sr and titanium Ti is used as the dielectric layer 13, and the BST layer is formed by a sol-gel method. The BST material is a material with a relatively large dielectric constant of 1500 as bulk, and thus it is effective for realizing a miniature capacitor with large capacitance.

[0051]

Specifically, an alkoxide starting solution is first used to form a BST layer by spin coating (2000 rpm/30 seconds). An approximately 100 nm thick film is obtained by one spin coating step under these spin coating conditions.

[0052]

The BST is then crystallized by prebaking for 10 minutes at a temperature of 400°C and main baking for 10 minutes at a temperature of 700°C, thereby forming a BST layer with a thickness of 100 nm, a dielectric constant of 300 and a dielectric loss of not more than 2%.

[0053]

The same sputtering method as that described above is used in the step of forming the upper electrode layer 14 shown in Fig. 2(D) to form a platinum Pt layer at a thickness of 100 nm as the upper electrode layer 14 on the BST dielectric layer 13.

[0054]

It is noted that as shown in Fig. 1, the sides of the capacitor 30 are formed in a stepwise fashion such that the edges of the lower layer extend outward beyond the edges of

the upper layer.

[0055]

By providing such stepwise extending sections, it is possible to stop fragments at the extending sections when fragments (particles) of the platinum material are produced during the fabrication process, thereby preventing adhesion of the fragments onto the sides of the dielectric layer and avoiding shorts between the electrodes.

[0056]

(ii) Lower electrode connection-forming step

An electrode connection-forming hole 21 from the lower electrode layer 12 is formed in the manner shown in Fig. 2(E).

[0057]

Specifically, a resist mask is formed by photolithography, and then the Pt of the upper electrode layer 14 and the BST layer of the dielectric layer 13 are dry etched in that order by argon Ar ion milling.

[0058]

(iii) Barrier layer-forming step

Next, as shown in Fig. 2(F), a barrier layer 15 is formed so as to cover the capacitor 30 (both the top and side thereof).

[0059]

Specifically, silicon nitride Si_3N_4 used as the material for the barrier layer 15 is formed at a thickness of about 150 μm by a sputtering method. As alternatives to silicon nitride Si_3N_4 for the material of the barrier layer 15 there may also be used aluminum oxide Al_2O_3, silicon oxide SiO_2 or the like.

[0060]

The sputtering conditions applied herein are a substrate temperature of 200°C, an RF power of 500 W, a gas pressure of 0.1 Pa and an Ar/N_2 ratio of 5/1.

[0061]

As described above, aluminum oxide Al_2O_3, silicon oxide SiO_2, silicon nitride Si_3N_4 and the like may be used as non-conductive inorganic materials for the barrier layer 15.

However, the material used herein preferably has a thermal expansion coefficient equivalent to that of the dielectric layer 13 in order to avoid problems such as interlayer peeling that occur due to mechanical stress under exposure to severe temperature fluctuations in the field.

[0062]

If the thermal expansion coefficient of the material constituting the barrier layer 15 and the thermal expansion coefficient of the material constituting the dielectric layer 13 are equivalent, it becomes possible to prevent peeling and the like due to warping between layers caused by differences in thermal expansion coefficients, and to obtain a thin layer capacitor with high reliability.

[0063]

Further, the material of the barrier layer 15 is preferably of the same composition as the material of the dielectric layer 13 of the capacitor, in order to achieve satisfactory adhesion with the dielectric layer 13 of the capacitor.

[0064]

By using the same composition for the material constituting the barrier layer 15 as the composition of the material constituting the dielectric layer 13, it becomes possible to guarantee satisfactory layer adhesion. Furthermore, it becomes possible to obtain a thin layer capacitor 20 having high reliability for the bonding surface between the dielectric layer 13 and the barrier layer 15 against mechanical stress.

[0065]

Furthermore, the material of the barrier layer 15 is preferably an amorphous material.

[0066]

Generally, a crystallized metal oxide is used for the dielectric layer 13 in order to obtain a high dielectric constant. However, since gaps exist between the individual crystal grains of the crystals, migration of hydrogen ions in

the crystals is facilitated. It is therefore effective to use an amorphous material, which is resistant to hydrogen ion migration, as the barrier layer 15 to prevent such hydrogen ion migration. A high blocking effect against hydrogen ions can be achieved by a construction using such a material.

[0067]

(iv) Protective insulating layer-forming step

A protective insulating layer 16 made of for example a polyimide resin is formed over the barrier layer 15 as shown in Fig. 2(G).

[0068]

First, a photosensitive polyimide varnish is spin coated at 3000 rpm for 30 seconds, to form a 4 μm thick layer. This is followed by heating (prebaking) for 10 minutes at a temperature of 60°C and then by exposure and development steps and heating (main baking) for 2 hours at a temperature of 400°C to form a 2 μm thick polyimide PI film.

[0069]

(v) Contact hole-forming step

Contact holes 19 are formed as shown in Fig. 2(H) to expose the lower electrode layer 12 and upper electrode layer 14.

[0070]

Specifically, a resist mask (not shown) is formed by photolithography, and then the silicon nitride Si_3N_4 film is dry etched by argon Ar ion milling to expose the top of the capacitor and the lower electrode layer.

[0071]

(vi) Electrode pad- and bump-forming step

As shown in Fig. 2(I), electrode pads 17 for connection of bumps with each electrode of the capacitor 30 are formed by sputtering and plating as under bump metals (UBM). Finally, as shown in Fig. 2(J), bumps 18 are formed on the previously formed electrode pads 17 as terminals for electrical connection with a circuit board.

[0072]

It is noted that solder is generally used as the material for the bumps 18, but solder materials can diffuse into the electrode pads 17 and react with the platinum Pt of the electrode layers, thereby altering the resistance value of the platinum. For this reason, the material for the electrode pads 17 is preferably chromium Cr, titanium Ti, copper Cu, nickel Ni or the like from the standpoint of avoiding the aforementioned solder corrosion and improving the solder wettability.

[0073]

The thin layer capacitor 20 shown in Fig. 1 is thus formed by the production process described above.

[0074]

In the thin layer capacitor 20 of Fig. 1, the polyimide resin (protective insulating layer 16) which is hygroscopic and releases moisture under prescribed conditions is physically separated from the capacitor 30. That is, since moisture released from the polyimide resin is blocked before it reaches the catalytic electrode while in a non-ionized state, the moisture released from the polyimide resin is prevented from reaching the catalytic platinum Pt (upper electrode layer 14) surface.

[0075]

Consequently, the problem of reduction of the metal oxide of the dielectric layer 13 at the interface between the upper electrode layer 14 and the dielectric layer 13 is avoided.

[0076]

A resin material such as polyimide which absorbs mechanical stress from bumps can therefore be used as the protective insulating layer 16 resin material, while preventing reduction of the metal oxide dielectric layer material by moisture released from the resin material. As a result, it is possible to provide a thin layer capacitor 20 with excellent high-frequency tracking performance and low deterioration of characteristics.

[0077]

(Comparative Experiment on Capacitor Characteristics)

The following is a comparative experimental result of the capacitor characteristics of thin layer capacitors, one using a barrier layer 15 and the other using no barrier layer 15.

[0078]

Fig. 4 is a drawing of the measurement circuit used for the experiment, and Fig. 5 is a pair of graphs showing the measurement results for the experiment.

[0079]

In this experiment, silicon nitride Si_3N_4 was used as the barrier layer 15, platinum Pt was used as the material for the lower electrode layer 12 and upper electrode layer 14, and BST was used as the dielectric material.

[0080]

First, a capacitor 30 was formed on a silicon substrate 11, a connecting forming hole 21 was formed for connection with the lower electrode layer 12 of the capacitor 30, and the resulting state was designated as the initial state. The capacitor characteristics were measured in the initial state (before forming the polyimide resin as the protective insulating layer 16), while the capacitor characteristics were also measured with and without formation of the barrier layer 15 (after formation of the polyimide resin as the protective insulating layer 16).

[0081]

The circuit construction shown in Fig. 4 was used for the measurement, with an alternating current voltage of 50 mV_{pp} applied to each electrode of the capacitor 30. A prescribed direct current voltage was simultaneously applied.

[0082]

Figs. 5(A) and 5(B) are graphs showing the results of this experiment. Fig. 5(A) shows the capacitance ($\mu F/cm^2$) characteristic with respect to applied voltage (V), and Fig. 5(B) shows the dielectric loss (%) characteristic with respect to applied voltage (V).

[0083]

In each graph, the dotted curve (a) represents the initial characteristic before formation of the polyimide resin as the protective insulating layer 16.

[0084]

The solid curve (b) represents the characteristic after formation of the polyimide resin as the protective insulating layer 16 for a thin layer capacitor with no barrier layer 15.

[0085]

The solid curve (c) represents the characteristic after formation of the polyimide resin as the protective insulating layer 16 for a thin layer capacitor having a barrier layer 15.

[0086]

As shown in Fig. 5(B), the thin layer capacitor with no barrier layer 15 exhibited an increase in dielectric loss (tanδ) after formation of the polyimide resin as the protective insulating layer 16. Consequently, as indicated by the curve (b) in Fig. 5(A), the thin layer capacitor with no barrier layer 15 exhibited a deterioration in capacitance after formation of the polyimide resin as the protective insulating layer 16.

[0087]

In contrast, even after formation of the polyimide resin, the thin layer capacitor with a barrier layer 15 exhibited no increase in dielectric loss or deterioration in capacitance compared to the initial state (before formation of the polyimide resin).

[0088]

Thus, by covering the capacitor 30 with a barrier layer 15 to prevent infiltration of hydrogen into the upper electrode layer 14, it is possible to inhibit deterioration in the characteristics of the dielectric material.

[0089]

(Second Embodiment)

A process for production of a thin layer capacitor according to a second embodiment of the invention will now be explained.

[0090]

The drawings for this embodiment are the same as for the first embodiment (Figs. 2 and 3).

[0091]

This embodiment accomplished formation of the dielectric layer 13 shown in Fig. 2(C) using a sputtering method (instead of a sol-gel method), in contrast to the first embodiment. Also, a BST material in an amorphous state having the same composition as that of the dielectric layer 13 was used as the barrier layer 15 for the step of forming the barrier layer 15 shown in Fig. 2(F).

[0092]

First, a silicon wafer is used as the silicon substrate 11, and a sputtering method is used to form films of titanium oxide TiO_2 (20 nm) and platinum Pt (100 nm) in that order on the silicon wafer, as shown in Figs. 2(A) to 2(D), in the same manner as the first embodiment. Iridium Ir may also be used as the lower electrode material.

[0093]

Sputtering of the BST in the step of forming the dielectric layer 13 may be accomplished, specifically, under the following conditions.

[0094]

The film is formed with a substrate temperature of 600°C, an Ar/O_2 ratio of 8/1, a gas pressure of 0.4 Pa and an RF power of 800 W, to obtain a dielectric layer with a BST film thickness of 100 nm, a dielectric constant of 400 and a dielectric loss of not more than 1%.

[0095]

A platinum Pt film (100 nm) is formed as an upper electrode layer 14 on the BST dielectric layer 13 by the same sputtering method as that described above (substrate temperature: 400°C).

[0096]

In the subsequent lower electrode connection-forming step shown in Fig. 2(E), the platinum Pt film serving as the upper

electrode layer 14 and the BST film serving as the dielectric layer 15 are dry etched in that order by argon Ar ion milling to form a connection to the lower electrode layer 12.

[0097]

In the barrier layer-forming step shown in Fig. 2(F), an amorphous BST thin film as a barrier layer 15 is formed at a thickness of 150 nm by sputtering. The conditions are a substrate temperature of 200°C, and Ar/O_2 ratio of 8/1, a gas pressure of 0.2 Pa and an RF power of 800 W. By forming the film at low temperature it is possible to avoid crystallization of the BST to obtain BST in an amorphous state.

[0098]

Then, in the steps shown in Figs. 2(G) to 2(J), after forming the protective insulating layer 16 using a photosensitive polyimide resin in the same manner as in the second embodiment, the electrode pads 17 and bumps 18 are formed to complete the thin layer capacitor 20.

[0099]

According to this embodiment, the barrier layer 15 and the dielectric layer 13 have the same composition and the material of the barrier layer 15 is in an amorphous state, such that the resulting thin layer capacitor 20 has high adhesion between the barrier layer 15 and dielectric layer 13, wherein the barrier layer 15 exhibits a high hydrogen ion blocking effect (i.e. a high reduction-resistant effect).

[0100]

Moreover, by forming the dielectric layer 13 of the BST material by sputtering, formation of the capacitor 30 is carried out entirely in a vacuum, thereby allowing the thin layer capacitor 20 to be fabricated by a simpler process.

[0101]

(Third Embodiment)

A thin layer capacitor according to a third embodiment of the invention will now be explained with reference to Figs. 6(A) and 6(B).

[0102]

Fig. 6(A) is a perspective view of a thin layer capacitor, and Fig. 6(B) is a cross-sectional view taken along line X-X' of Fig. 6(A).

[0103]

This embodiment is an application example of a thin layer capacitor according to the first embodiment, and as shown in Fig. 6(A), a plurality of bumps are arrayed as terminals for the thin layer capacitor on one side of the thin layer capacitor. The plurality of bumps 18 are arranged such that adjacent bumps are connected to different electrodes of the capacitor 30.

[0104]

Specifically, each bump is electrically connected to every other electrode, and the connected capacitors 30 are internally connected together, as shown in Fig. 6(B).

[0105]

For external connection of each bump, a bump 18a is connected to the power line of a circuit board (not shown), while a bump 18b is electrically connected to each GND line of the circuit board. The power and GND lines of the circuit board are in turn connected to an LSI or the like (not shown) mounted on the circuit board.

[0106]

Thus, in this thin layer capacitor 20, the terminals with the circuit board on which the thin layer capacitor 20 is mounted are not limited to the edges of the package but are also provided at the center section of the package.

[0107]

Consequently, even when the capacitor 30 inside the thin layer capacitor 20 has a large form, the terminals may be provided at any desired location at the center of the package to reduce the spaces between power-GND terminals and achieve narrow wiring spaces over the entire area of power and GND wiring which connects the LSI and thin layer capacitor.

[0108]

In other words, the thin layer capacitor 20 has high capacitance and is capable of low inductance connection (the high-frequency characteristics are improved), and thus is suited for the optimum conditions for a decoupling capacitor.

[0109]

According to this embodiment, therefore, it is possible to provide a thin layer capacitor with high capacitance and excellent high-frequency characteristics.

[0110]

(Fourth Embodiment)

A thin layer capacitor according to a fourth embodiment of the invention will now be explained with reference to Fig. 7.

[0111]

Fig. 7 is a view from the top of the thin layer capacitor, wherein reference numeral 31 indicates the capacitor area for the capacitors 30.

[0112]

This embodiment is an application example of a thin layer capacitor according to the third embodiment, and as shown in Fig. 7, a plurality of capacitors 30a, 30b, 30c with different sizes are arranged on one thin layer capacitor 20.

[0113]

The capacitance of each capacitor is generally in proportion to the area occupied by the capacitor. For example, capacitor "b" occupies twice the area of capacitor "a", and has a capacitance of approximately twice that of capacitor "a".

[0114]

With this construction, for example, when a plurality of capacitors with different capacitances are necessary, it is sufficient to mount a single package instead of mounting a plurality of thin layer capacitors, thereby allowing more efficient use of the mounting area on the circuit board (not shown) on which the thin layer capacitor 20 is mounted.

[0115]

Additional effects that may be expected with this embodiment include reduced cost of parts for decoupling capacitors and fewer mounting steps for mounting of parts.

[0116]

The preferred embodiments of the invention will be summarized as follows.

[0117]

(Appendix 1) A thin layer capacitor comprising a capacitor with a dielectric layer made of a metal oxide and a protective insulating layer made of a resin material, characterized in that a barrier layer made of a non-conductive inorganic material is provided between the capacitor and the protective insulating layer.

[0118]

(Appendix 2) A thin layer capacitor characterized by comprising:

a capacitor with a dielectric layer made of a metal oxide, formed on a supporting substrate;

a barrier layer made of a non-conductive inorganic material covering at least the top and side of the capacitor; and

a protective insulating layer made of a resin material, formed on the barrier layer.

[0119]

(Appendix 3) A thin layer capacitor as described in Appendix 1 or 2, characterized in that the barrier layer is a material having the same thermal expansion coefficient as that of the dielectric layer.

[0120]

(Appendix 4) A thin layer capacitor as described in Appendix 1 or 2, characterized in that the barrier layer has the same composition as that of the dielectric layer.

[0121]

(Appendix 5) A thin layer capacitor as described in Appendix 1 or 2, characterized in that the barrier layer is aluminum oxide, silicon oxide or silicon nitride.

[0122]

(Appendix 6) A thin layer capacitor as described in any one of Appendices 1 to 5, characterized in that the barrier layer is amorphous.

[0123]

(Appendix 7) A thin layer capacitor as described in any one of Appendices 1 to 6, characterized in that used as the material of the dielectric layer is a composite oxide comprising at least one of strontium, barium, lead, zinc, bismuth, tantalum, titanium, magnesium and niobium.

[0124]

(Appendix 8) A thin layer capacitor as described in any one of Appendices 1 to 7, characterized in that the sides of the capacitor have a stepwise fashion such that the edges of the lower layer extend outward beyond the edges of the upper layer.

[0125]

(Appendix 9) A thin layer capacitor as described in any one of Appendices 1 to 8, characterized in that the terminals for external electrical connection are provided at least at a location other than the edge of one side of the package.

[0126]

(Appendix 10) A thin layer capacitor as described in Appendix 9, characterized in that the electrode pads connecting the terminals and capacitor are supported by the protective insulating layer.

[0127]

(Appendix 11) A thin layer capacitor as described in any one of Appendices 1 to 10, characterized in that a plurality of capacitors with different capacitances are provided in a single thin layer capacitor.

[0128]

(Appendix 12) A process for production of a thin layer capacitor comprising a capacitor with a dielectric layer made of a metal oxide and a protective insulating layer made of a resin material, characterized by comprising the steps of:

forming the capacitor;

forming a barrier layer made of a non-conductive inorganic material, situated between the capacitor and the protective insulating layer; and

forming the protective insulating layer situated on the barrier layer.

[0129]

(Appendix 13) A process for production of a thin layer capacitor characterized by, comprising the steps of:

forming a capacitor with a dielectric layer made of a metal oxide, formed on a supporting substrate;

forming a barrier layer made of a non-conductive inorganic material covering at least the top and side of the capacitor; and

forming a protective insulating layer made of a resin material, formed on the barrier layer.

[0130]

(Appendix 14) A process for production of a thin layer capacitor as described in Appendix 13, characterized in that the step of forming the dielectric layer is accomplished by a sputtering method.

[0131]

[Effect of the Invention]

As explained in detail above, the thin layer capacitor of the invention comprises a capacitor with a dielectric layer made of a metal oxide and a protective insulating layer made of a resin material, in a construction wherein a barrier layer made of a non-conductive inorganic material is provided between the capacitor and the protective insulating layer.

[0132]

As a result of this construction, a resin material such as polyimide which absorbs the mechanical stress from bumps may be used as the protective insulating layer, while reduction of the metal oxide dielectric layer material by moisture released from the resin material is prevented. It is thereby possible to provide a thin layer capacitor which has

excellent high-frequency tracking performance and low deterioration of characteristics.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[Fig. 1]

Fig. 1 is a cross-sectional view of a thin layer capacitor according to the first embodiment of the invention.

[Fig. 2]

Fig. 2 is a cross-sectional view showing the steps of a production process for a thin layer capacitor according to the first embodiment of the invention.

[Fig. 3]

Fig. 3 is a cross-sectional view showing the steps of a production process for a thin layer capacitor according to the first embodiment of the invention.

[Fig. 4]

Fig. 4 is a drawing of the measurement circuit used in a capacitor characteristic measuring experiment for a thin layer capacitor of the invention.

[Fig. 5]

Fig. 5 is a pair of graphs showing the measurement results of a capacitor characteristic measuring experiment for a thin layer capacitor of the invention.

[Fig. 6]

Fig. 6 is a perspective view and cross-sectional view of a thin layer capacitor according to the third embodiment of the invention.

[Fig. 7]

Fig. 7 is a full constitutional drawing as seen from the top of a thin layer capacitor according to the fourth embodiment of the invention.

[Fig. 8]

Fig. 8 is a series of cross-sectional views showing the steps of a prior art production process for a thin layer capacitor.

[Fig. 9]

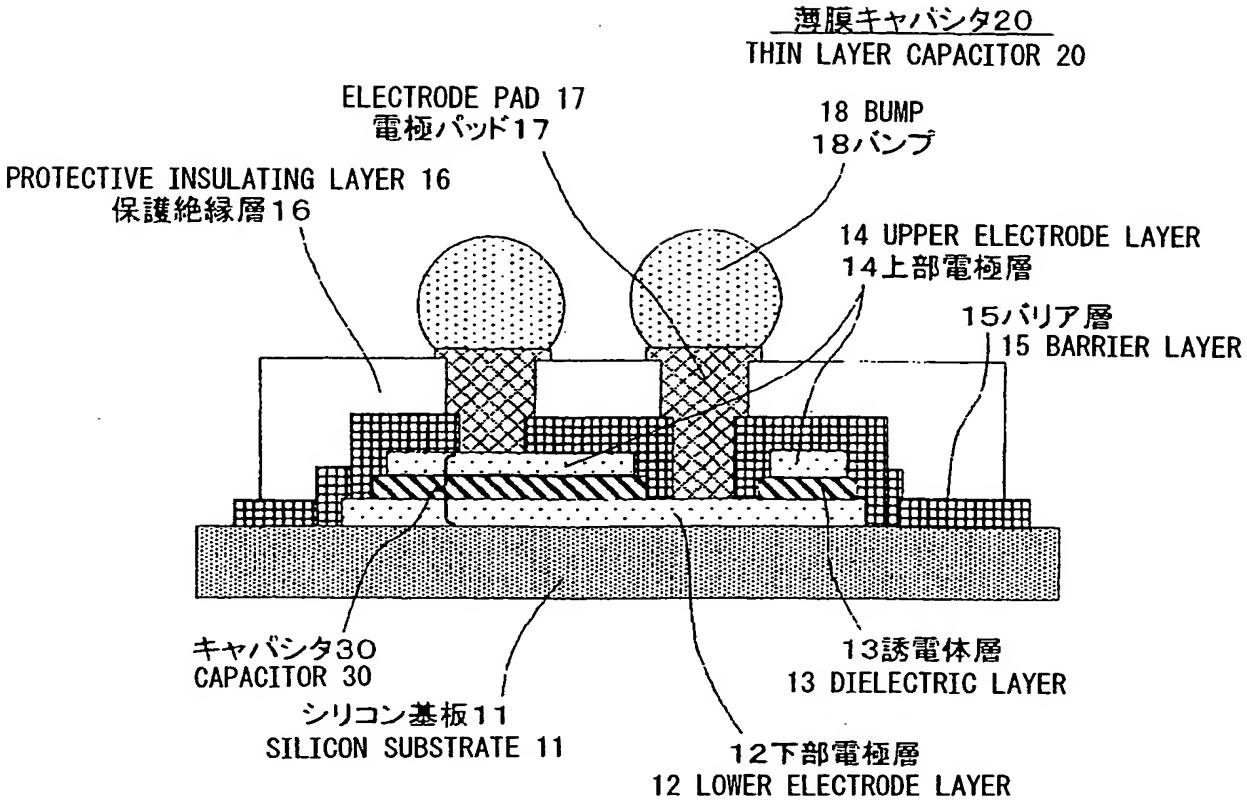
Fig. 9 is a series of cross-sectional views showing the steps of a prior art production process for a thin layer capacitor.

[Explanation of Reference Numerals]

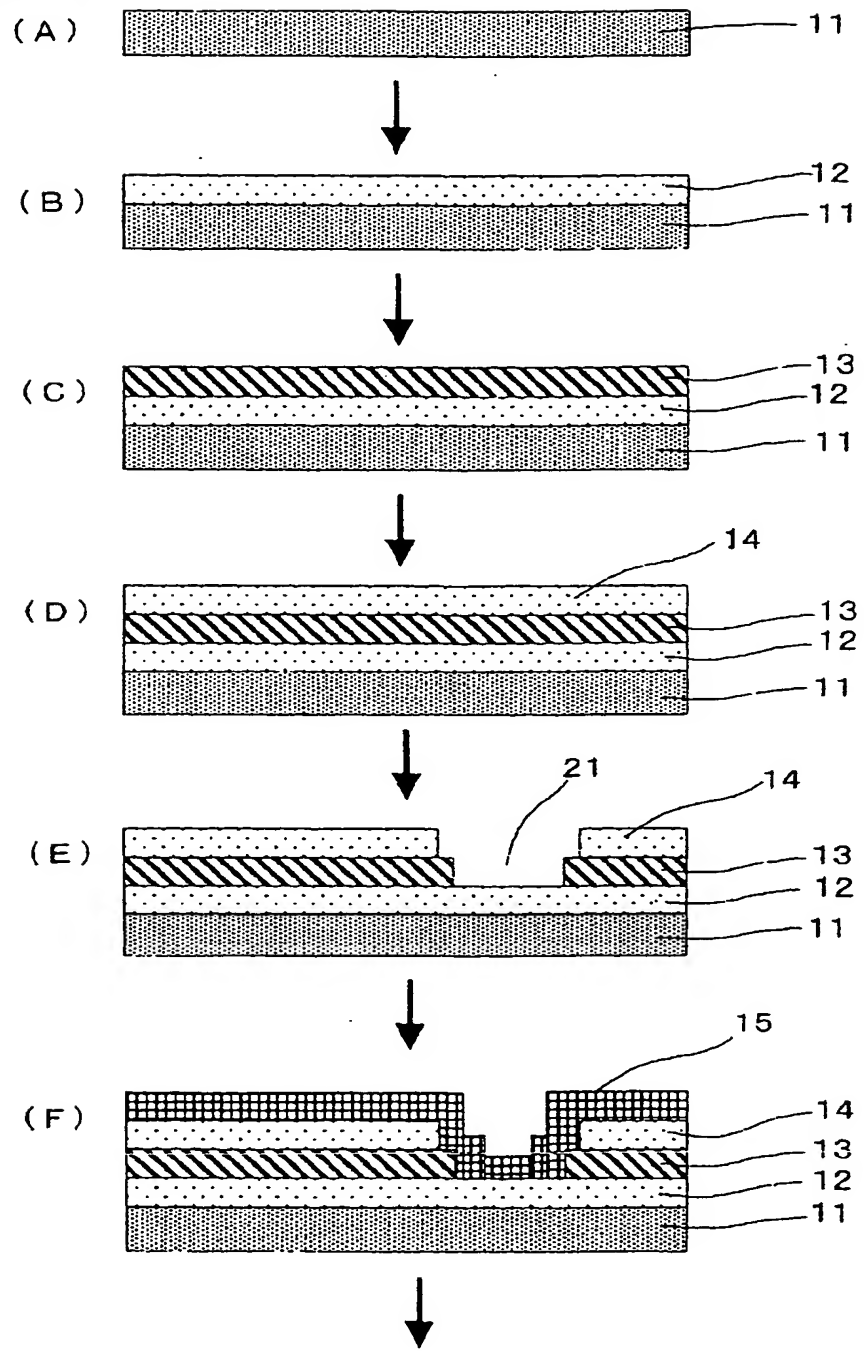
1: semiconductor substrate
2: lower electrode
3: capacitive insulating layer
4: upper electrode
6: protective insulating layer
9: contact holes
10: resist mask
11: silicon substrate
12: lower electrode layer
13: dielectric layer
14: upper electrode layer
15: barrier layer
16: protective insulating layer
17: electrode pad
18: bump
18a: bump connected to power line
18b: bump connected to GND line
19: contact holes
20: thin layer capacitor
21: electrode connection-forming hole
30: capacitor
30a: capacitor a
30b: capacitor b
30c: capacitor c
31: capacitor area

[NAME OF DOCUMENT] DRAWINGS
【書類名】 図 面

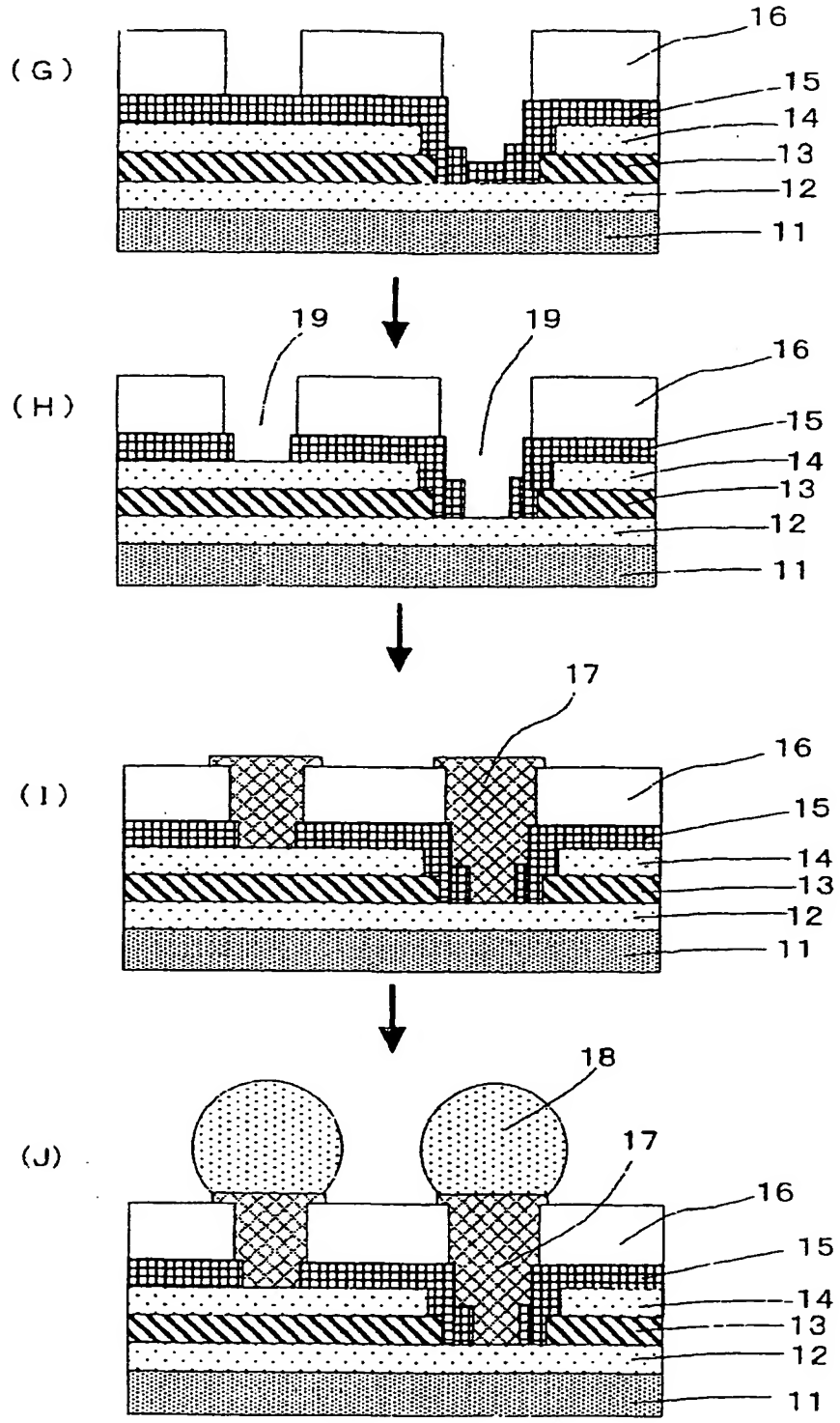
【図１】
[FIG. 1]



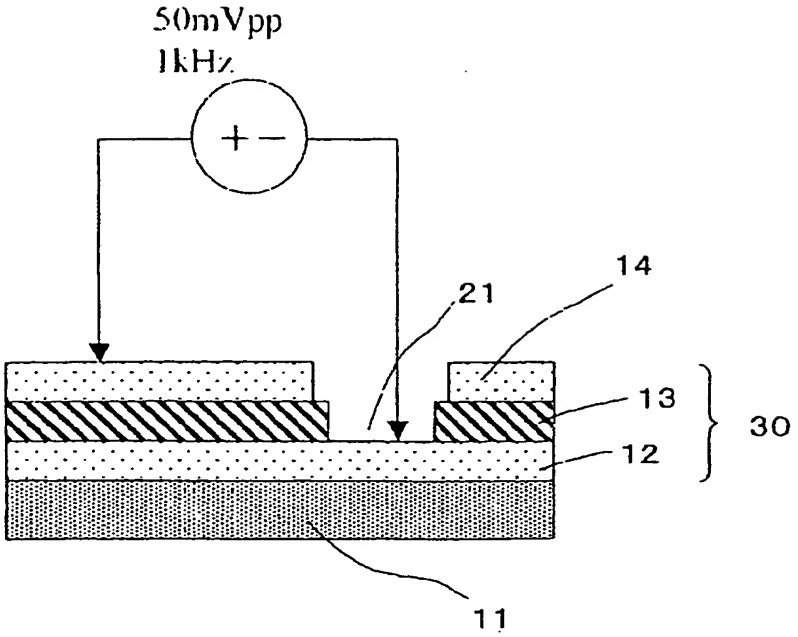
【図２】
[FIG. 2]



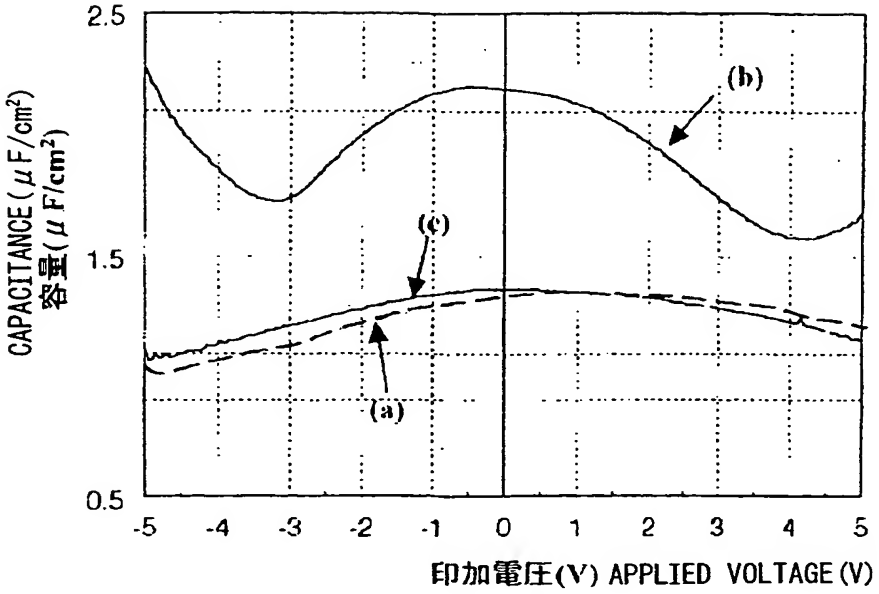
【図３】
[FIG. 3]


(G)
16
15
14
13
12
11
(H)
19
19
16
15
14
13
12
11
(I)
17
16
15
14
13
12
11
(J)
18
17
16
15
14
13
12
11

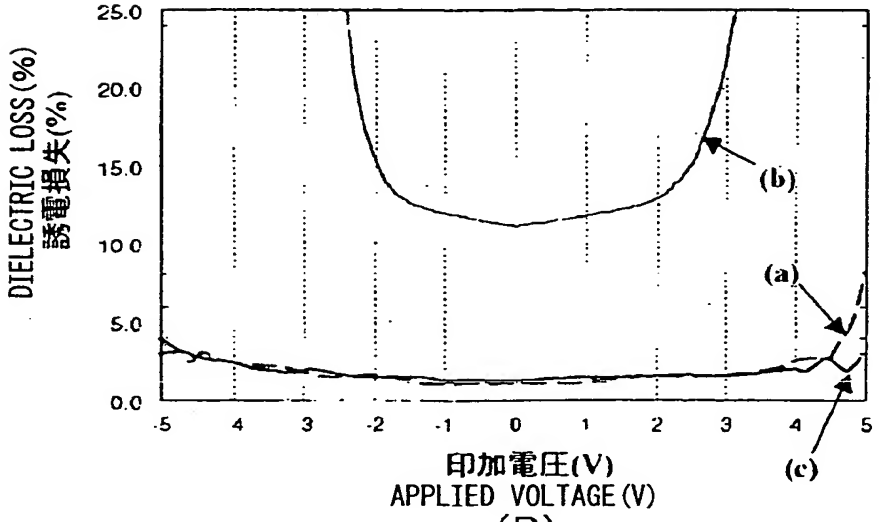
【図４】
[FIG. 4]



【図５】
[FIG. 5]

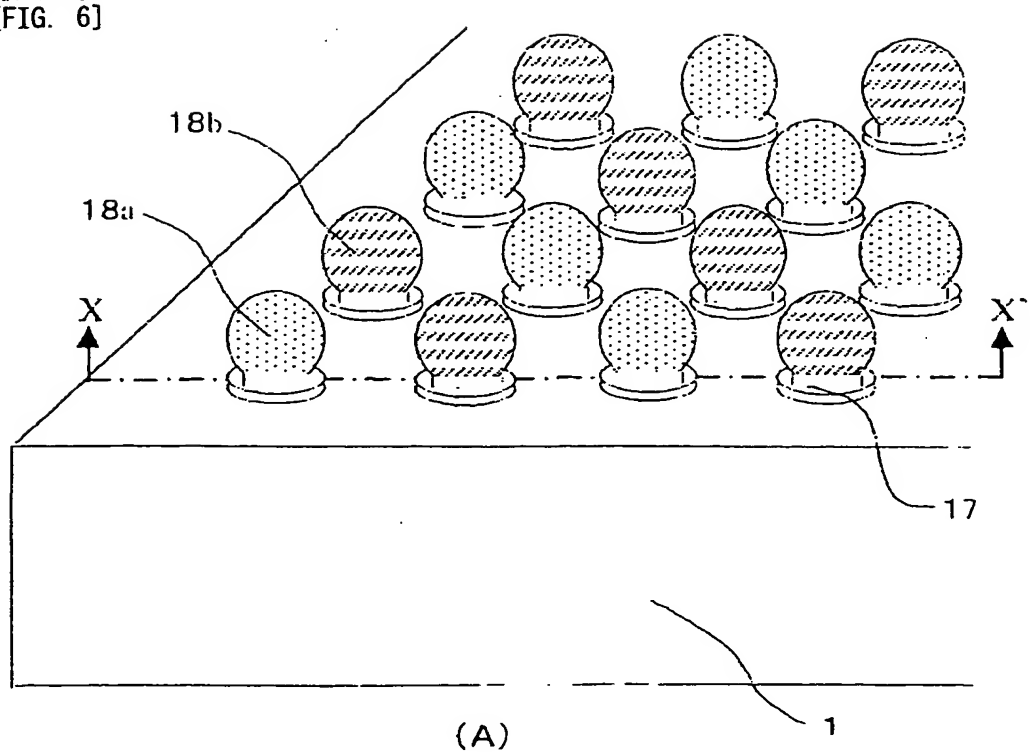

2.5
1.5
0.5
CAPACITANCE(μF/cm²)
容量(μF/cm²)
(b)
(c)
(a)
-5 -4 -3 -2 -1 0 1 2 3 4 5
印加電圧(V) APPLIED VOLTAGE(V)

(A)

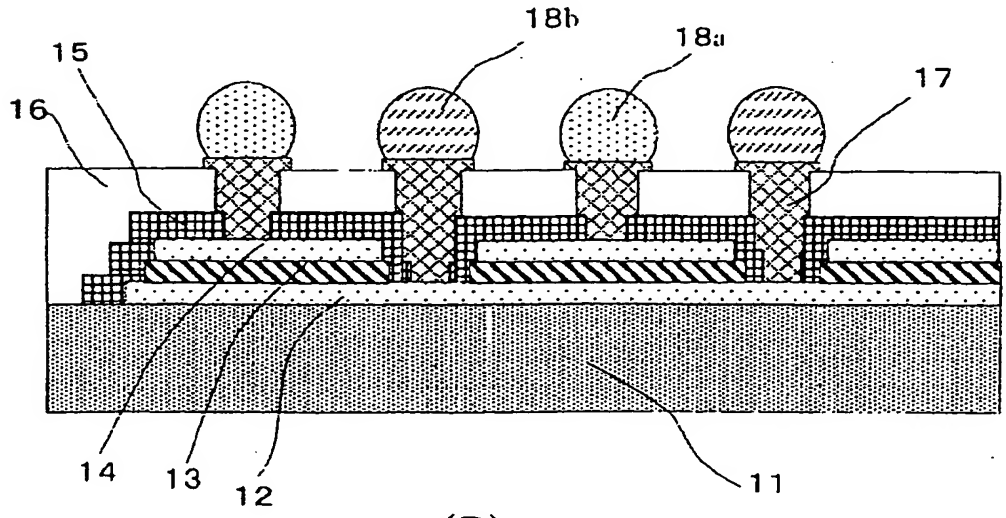

25.0
20.0
15.0
10.0
5.0
0.0
DIELECTRIC LOSS(%)
誘電損失(%)
(b)
(a)
(c)
-5 4 3 -2 -1 0 1 2 3 4 5
印加電圧(V)
APPLIED VOLTAGE(V)

(B)

【図６】
[FIG. 6]

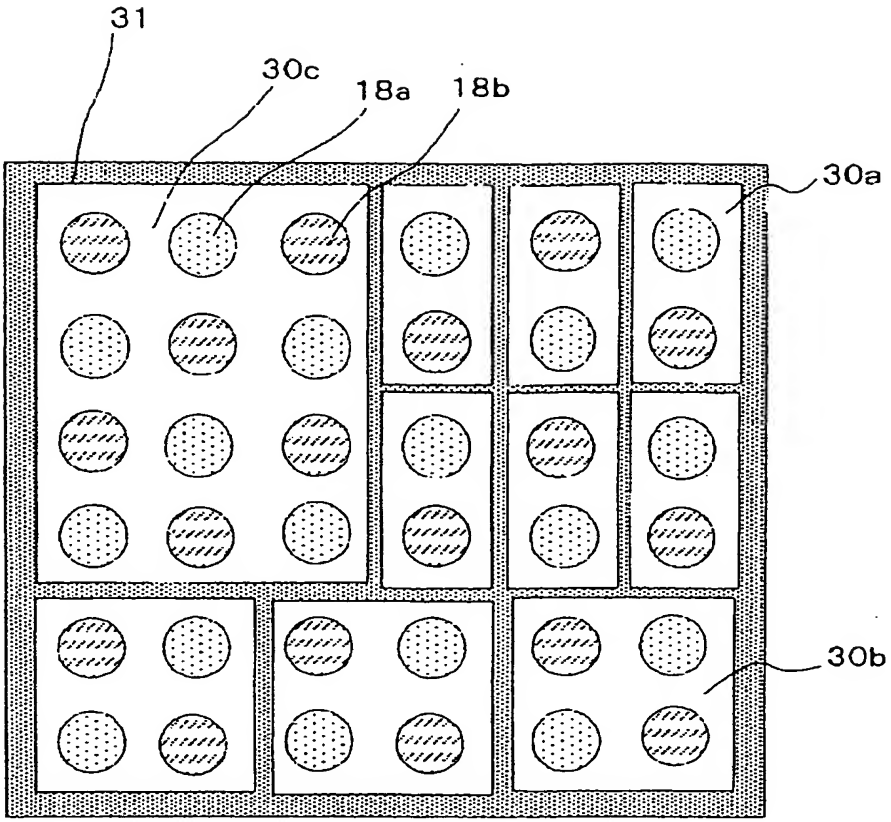


(A)

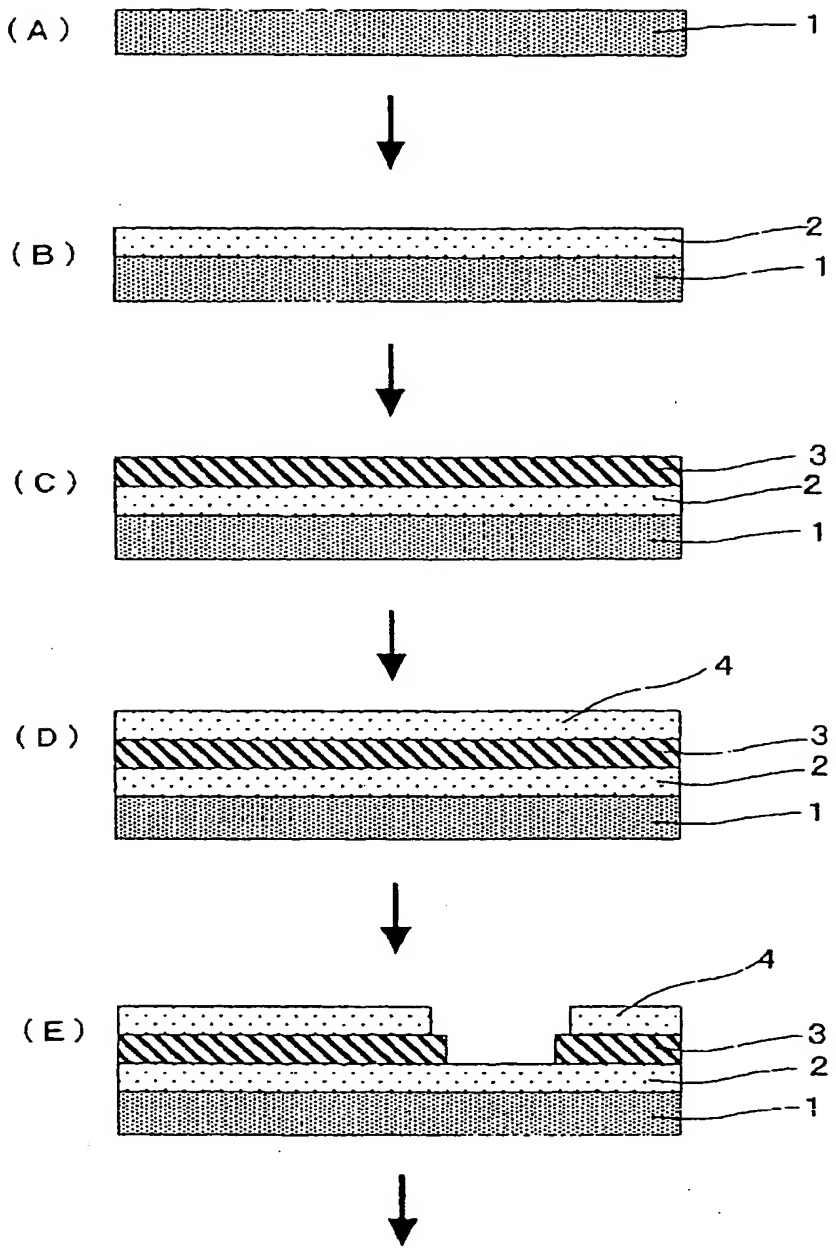


(B)

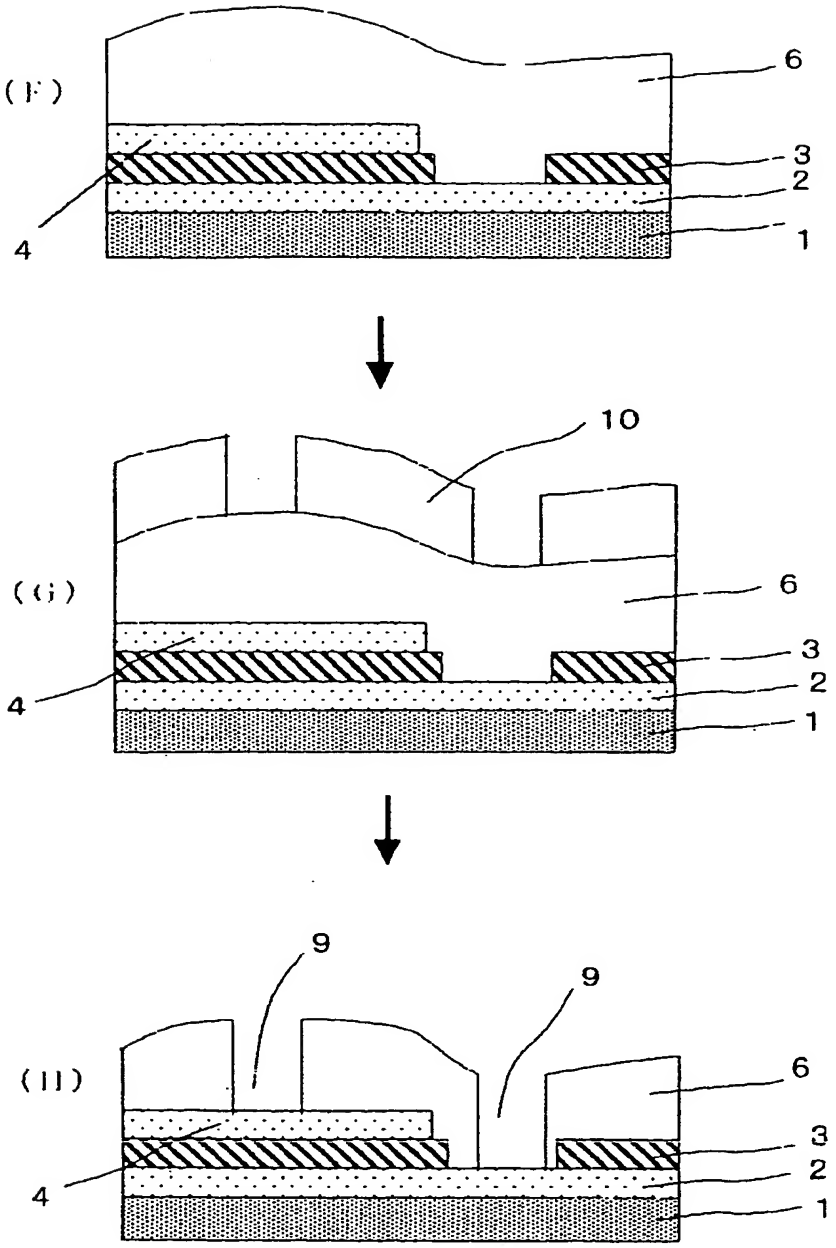
【図７】
[FIG. 7]



【図８】
[FIG. 8]



【図９】
[FIG. 9]



[NAME OF DOCUMENT] Abstract

[SUMMARY]

[OBJECT]

To provide a thin layer capacitor which avoids reduction of the dielectric material which occurs when a resin material such as polyimide which absorbs the mechanical stress from bumps is used as a protective insulating layer, and which has excellent high-frequency tracking performance and low deterioration of characteristics.

[SOLUTION MEANS]

In a thin layer capacitor comprising a capacitor having a dielectric layer made of a metal oxide and a protective insulating layer made of a resin material, a barrier layer made of a non-conductive inorganic material is provided between the capacitor and the protective insulating layer.

[SELECTED DRAWING] Fig. 1